reprinted from 4 April 1965 issue of
Electronics
a McGraw-Hill publication

2½-D memory operates in nanoseconds

Computer memory's unusual wiring scheme permits high-speed operation at low cost

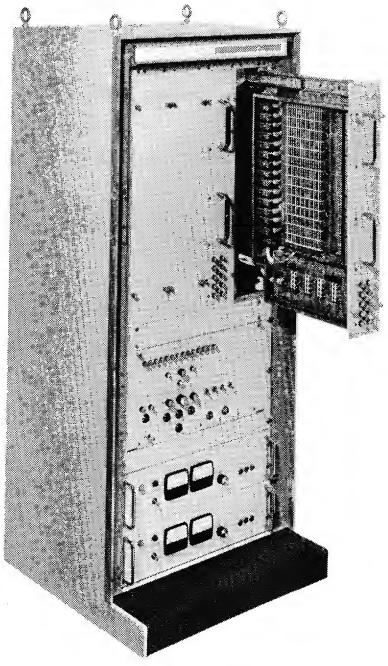
The world's fastest large-scale commercially available ferrite-core memory will make its debut at the Spring Joint Computer Conference in Boston, April 26 to 28. The Nanomemory 650, made by Electronic Memories, Inc., has a cycle time of 650 nanoseconds and an access time of 300 nanoseconds, for any of up to 16,384 words each of which may be as long as 84 bits.

This speed is attained with a 2½-dimensional organization, which combines the speed of a linear-select, or 2-D, design with the economy of a coincident-current, or 3-D, design. The cores are toroidal, similar to those in most conventional ferrite-core memories, with an outside diameter of 0.02 inch. The memory is faster than other big ferrite-core memories, and bigger than other fast memories, some of which are experimental only. [See p. 118; and Electronics, Dec. 28, 1965, p. 36, for example.]

The sketch below illustrates how the 2½-D combines the advantages of its 2-D and 3-D cousins.

A 2-D memory is organized as a single plane. It is expensive because, for high speed, a capacity of 2^n words requires decoding of n address bits.

Because a 3-D organization requires substantially less address decoding it is cheaper, but it is substantially slower. It is organized as a series of stacked planes; each plane contains one bit in each word contained in the memory.



In the 2½-D organization, the plane array resembles the 2-D; but the x-winding is doubled around to pass through two rows of cores. Current in the x-winding may pass in one direction or the other, depending on which of the two rows of cores is being addressed.

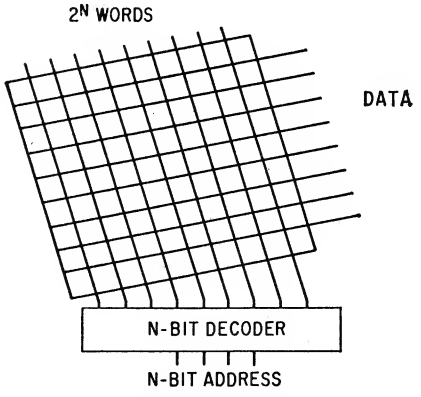
The Nanomemory 650 is complete with all electronic circuits in one package. However, only one side of the data register is available as output; if the user requires both 0 and 1 outputs, he must provide his own inverters in his own circuit package.

A price range of 6 to 8 cents per bit is quoted for the N-650. This comes to about $100,000 for the largest available size, 16,384 words by 84 bits.

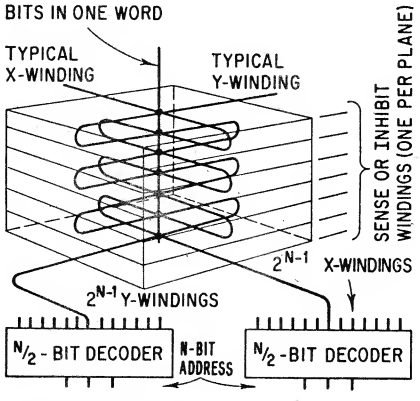
Specifications

Capacity	4,096, 8,192, or 16,384 words
Word length	8 to 84 bits
Operations	Read and restore Clear and write Read, modify and write (split cycle)
Cycle time	650 nanoseconds (read, write) 775 nanoseconds (minimum split)
Access time	300 nanoseconds
Input power	115 ±10 vac, 60 cps, single phase, 3 wire 700 watts normal, 1700 peak, typical (varies with word length)
Operating environment	+10° to +40° C., 90% relative humidity
Interface	Twisted-pair, either voltage or current. Either positive or negative voltage output (not both)
Weight	350 pounds
Delivery	4½ to 5 months

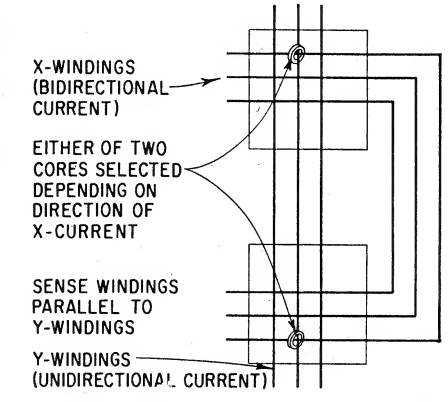
Electronic Memories, Inc., 12621 Chadron Ave., Hawthorne, Calif. 90250
Circle **350** on reader service card.



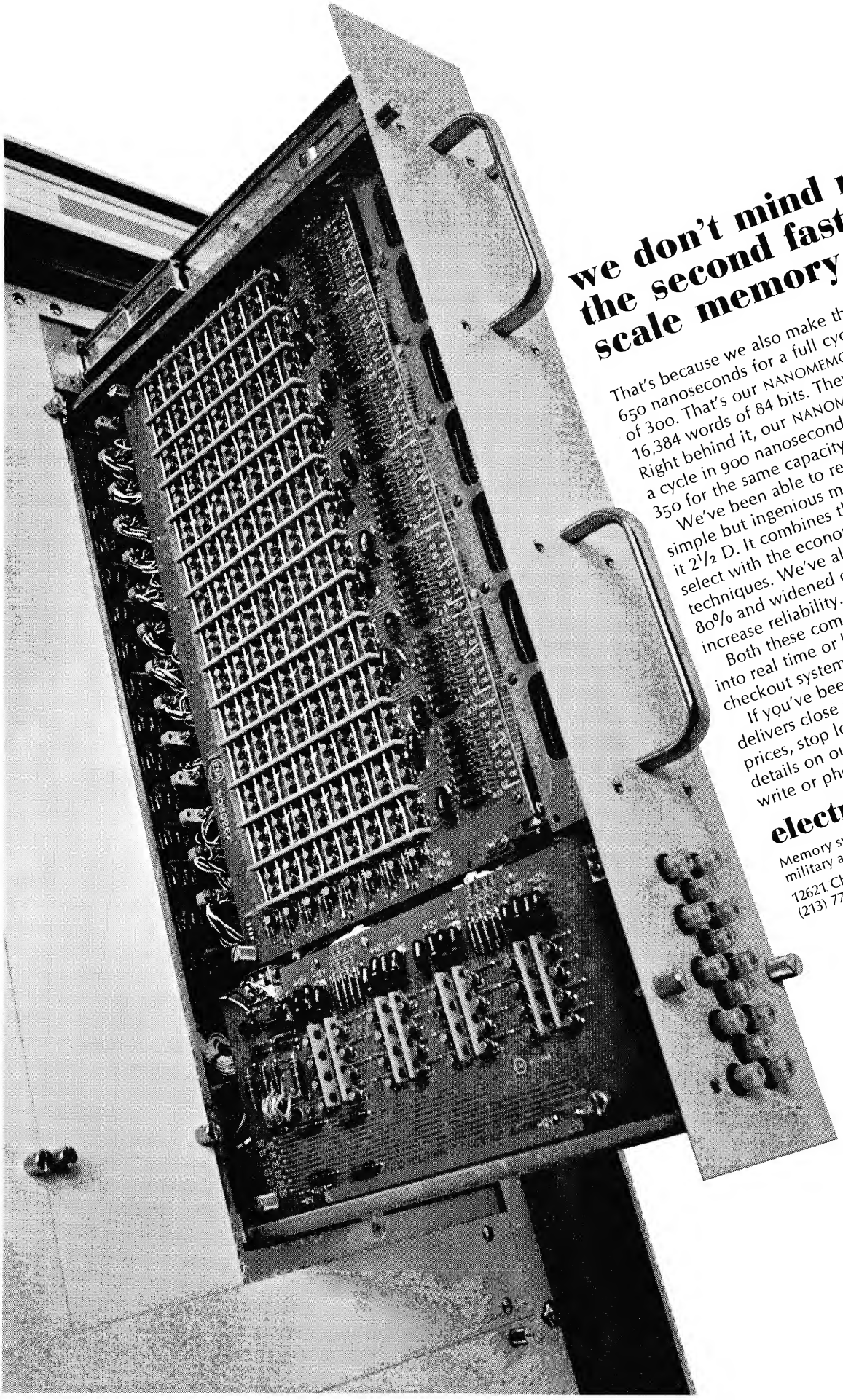
Two-dimensional organization is fast but quite expensive for large memories.



Three-dimensional organization is less expensive, but limited in speed.



Bidirectional current is part of address decoding in 2½-dimensional scheme.



we don't mind making the second fastest large scale memory system.

That's because we also make the fastest. How fast? 650 nanoseconds for a full cycle with an access time of 300. That's our NANOMEMORY(TM) 650. It handles up to 16,384 words of 84 bits. They don't come any faster. Right behind it, our NANOMEMORY 900 completes a cycle in 900 nanoseconds with an access time of 350 for the same capacity.

We've been able to reach these speeds by using a simple but ingenious magnetic organization. We call it 2½ D. It combines the speed potential of linear select with the economy of coincident current techniques. We've also reduced stack connections by 80% and widened operating margins to increase reliability.

Both these compact memory systems fit perfectly into real time or high speed computers and checkout systems.

If you've been looking for a memory system that delivers close to thin film speeds at magnetic core prices, stop looking. We've got two. For complete details on our NANOMEMORY 650 or 900, write or phone

electronic memories

Memory systems, stacks and cores for commercial, military and space applications
12621 Chadron Avenue, Hawthorne, California
(213) 772-5201

EMI 6176 4/66 1.5M

REPRINTED BY NEREM FROM THE NEREM RECORD 1965, A DIGEST OF PAPERS PRESENTED AT THE NORTHEAST ELECTRONICS RESEARCH AND ENGINEERING MEETING ON NOVEMBER 3, 4 and 5, 1965

SESSION: Circuits for Digital Computers

TAM-5: Comparison of Ferrite Core Memory Systems

T. J. Gilligan and **P. B. Persons**
Electronic Memories, Inc.
Hawthorne, California

A RECENTLY INTRODUCED memory system organization is shown in Figure 1. It has been called a two and a half dimensional (2-1/2 D) system and will be compared to a two dimensional (2 D) linear select system and a three dimensional (3 D) coincident current system.

It has been called 2-1/2 D because it falls somewhere between linear select and coincident current in decoding efficiency and, therefore, in parts count. Figure 1 shows the organization of the 2-1/2 D system. The significant points are:

1. The array is basically planar, i.e. selection is made in two coordinates.
2. The selection is completely redundant on a bit basis, i.e. each bit has a separate decode matrix on one-half select current.
3. There are two intersections of active drive lines per bit where the currents are coincident in one and anti-coincident in the other, the selected core being determined by the phasing of the word current.

Figures 2, 3, and 4 show block diagrams of the 3 D, 2 D, and 2-1/2 D systems respectively. Included in the blocks are the number of elements and the weighting (K) of that element. The cost equations and the pertinent drive information are included in the figures.

SPEED CAPABILITIES—In smaller systems, the linear select approach offers the most promise for high speed since:

1. With two wires, a smaller and, therefore, a faster core may be used.
2. Overdrive on read is feasible since readout is not achieved by current coincidence and further, expensive parts may be used.
3. Partial switching may be used.
4. Bipolar digit current may be used and, thereby, overdrive on write.
5. Since the magnetics array is small, the propagate and recovery effects will be minimized.

In larger systems of the present main memory class, 2-1/2 D is the most attractive solution since:

1. Higher drive and, therefore, faster switching cores than in the 2 D approach may be used, however, the core would be somewhat larger. The drive is limited in a 2 D system since the read diodes must handle full read current and, therefore, would be expensive for high drive cores.
2. There are no digit recovery problems, since the drive lines are short and further, the maximum intersection of a drive and a sense line is small.
3. Less time has to be allowed between the read and write beats of a cycle (as compared to a 3 D approach) due to the fact that an additive rather than an inhibitive digit is used. For the same drive voltage, faster rise times are possible, since the drive lines represent less of a load. Also, the propagate times are shorter than an equivalent 2 D and 3 D systems.

COST—The cost per bit of a coincident current system is relatively independent of system configuration, and is a good compromise for any memory system. In the faster systems, the 3-wire coincident current would be somewhat cheaper than the 4-wire, but would have the same slopes in the figure.

The cost of a linear select system is strongly a function of the number of bits per word. This could be expected since for every word we have to mount a pair of diodes and handle two wire ends.

Linear select has been used for shorter word lengths by letting a memory word equal a number of computer words and "spinning" the selected, but not used information. This allows more cores per drive line, but requires more sense amps.

The cost of a 2-1/2 D 3-wire system is strongly influenced by the number of words. This is so because the last level of electronic decoding accounts for a significant percentage of the total system cost and an improved efficiency here will strongly affect the system cost.

It's interesting to note that a 2-wire 2-1/2 D system may be made to run at a microsecond in the half million bit area using 20 mil cores, however, the cost crossover with a 3-wire 2-1/2 D system is at about 32 K. This is because the decoding requirements increase for a 2-wire system in order to drive balanced currents for sensing.

In Figure 5, the loci of equal costs are shown for the three systems. These are approximate and will be significantly affected by the particular design.

THROUGHPUT PER DOLLAR—As memories get larger, the magnetics assumes a more important percentage of the system cost and it is in this area where linear select becomes important. If the computer can use multiple words, a linear select system may achieve very high data rates at a reasonable cost.

FLEXIBILITY—Of major concern to a memory manufacturer is the flexibility of the system or the ability to meet many different customer requirements easily and maintain commonality of parts. This is naturally less important to a computer manufacturer who designs his own memory. The coincident current approach is clearly superior in this regard since:

1. The cost per bit is almost constant over a large range of requirements.
2. It is extremely simple to add or subtract bits from the basic design.

Linear select is very poor since the matrix frame must contain the whole word, and, therefore, should be strung for the maximum length word.

The 2-1/2 D approach is inherently flexible since a bit may be added complete with its drive and sense circuitry, however, this will be compromised to optimize manufacturing costs.

RELIABILITY AND POWER—These are items that are important in both commercial and military applications. The 2-1/2 D system offers promise as a low power system since the bit line inductance and D. C. resistance are low, requiring a minimum of power to get current up and then to maintain it. It also doesn't need as fast a rise time to match the performance of the other systems.

The 2-1/2 D system utilizes a planar organization and, therefore, wire ends and in turn solder joints may be significantly reduced. The disadvantage is that since the parts count is high, reliability will suffer below 32 K words. This is partially offset by the lower stress levels on all components.

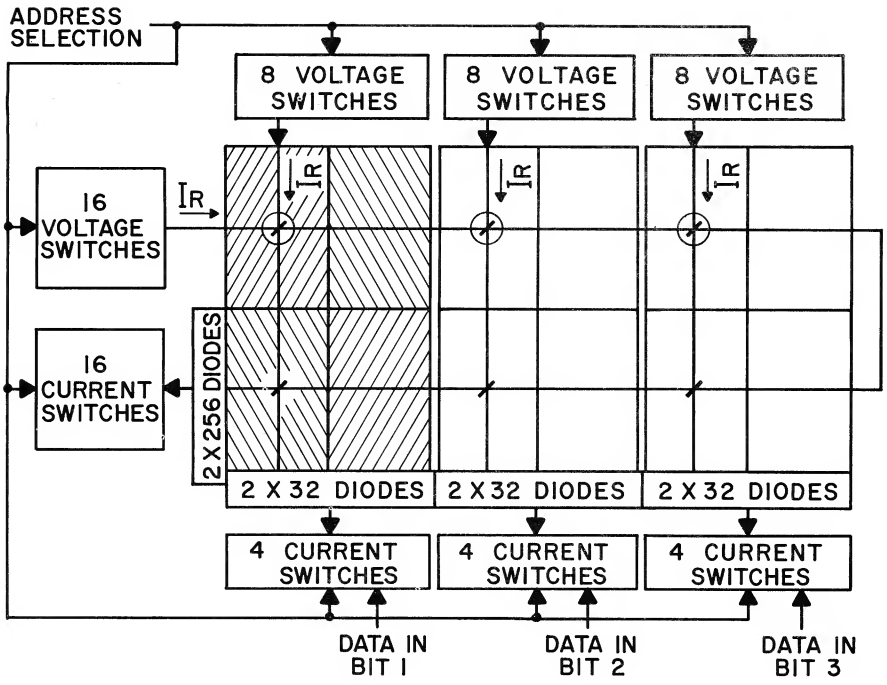
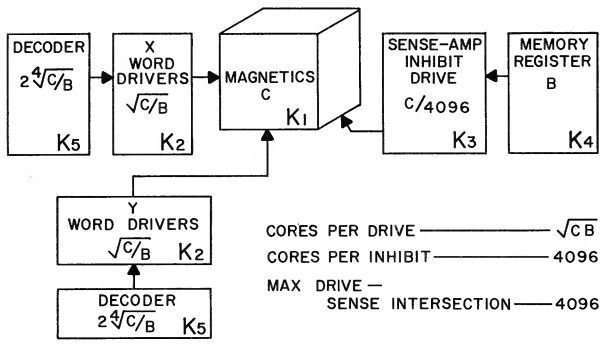


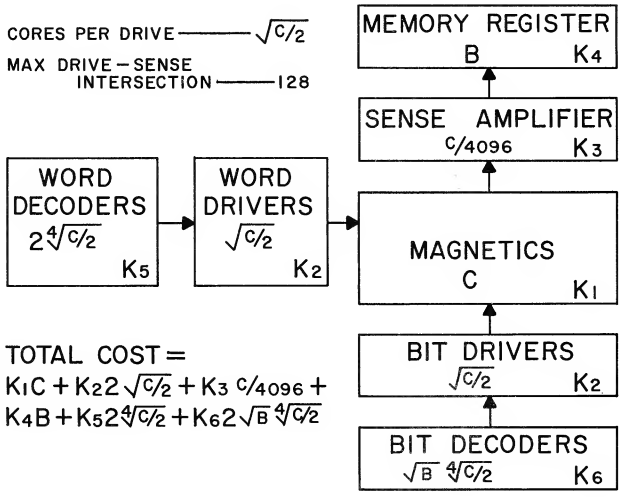
FIGURE 1—16K x 3 BIT 2-1/2 D MEMORY ORGANIZATION. 256 horizontal phased word lines and 32 vertical bit lines define 16,384 addresses. The bit decoding is duplicated for every bit.



TOTAL COST =

$$K_1C + K_2 2\sqrt{C/B} + K_3\, C/4096 + K_4B + K_5 4\sqrt[4]{C/B}$$

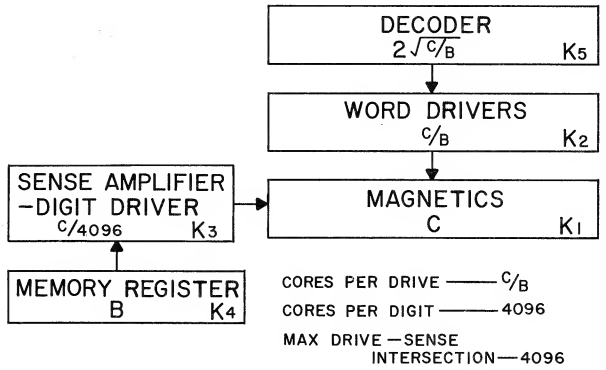
FIGURE 2—COINCIDENT CURRENT (3 D) BLOCK DIAGRAM. This system is characterized by a cubic magnetics array and a relatively small number of word drivers and associated decoding.



TOTAL COST =

$$K_1C + K_2 2\sqrt{C/2} + K_3\, C/4096 + K_4B + K_5 2\sqrt[4]{C/2} + K_6 2\sqrt{B}\sqrt[4]{C/2}$$

FIGURE 4—2-1/2 D BLOCK DIAGRAM. This system is planar and also square, the word drivers are minimized for a planar array but are still more than required for a cubic array.



TOTAL COST = $K_1C + K_2\frac{C}{B} + K_3\frac{C}{4096} + K_4B + K_5 2\sqrt{C/B}$

FIGURE 3—LINEAR SELECT (2 D) BLOCK DIAGRAM. This system is planar, but basically rectangular having a large number of word drivers.

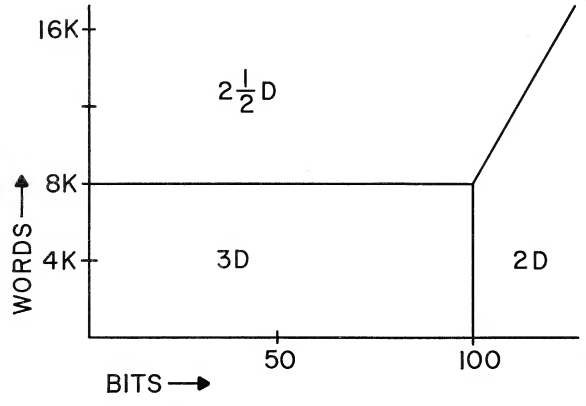


FIGURE 5—LOCI OF APPROXIMATE EQUAL COST. Each of the three approaches tends to be more efficient in the domains shown. The loci of equal costs will depend on the particular design.